2	1.	(Original) A method of forming a capacitor on a semiconductor substrate, the method					
3		inclu	including the steps of:				
4		(a)	forming a device body in the semiconductor substrate using a first type of dopant				
5	,		material;				
6		(b)	forming a dielectric layer over the device body;				
7		(c)	forming an electrode layer over the dielectric layer in an area defined by an upper				
8	•		surface of the device body;				
9		(d)	forming a first lateral region in the semiconductor substrate along a first lateral				
10			side of the device body, the first lateral region being in electrical contact with the				
11			device body along the first lateral side of the device body and containing the first				
12	•	.,	type of dopant material at a level relatively higher than is characteristic of the				
13		,	device body;				
14	`.	(e)	forming a second lateral region in the semiconductor substrate along a second				
15			lateral side of the device body opposite the first lateral side, the second lateral				
16	•		region being in electrical contact with the device body along the second lateral				
17			side of the device body and containing the first type of dopant material at a level				
18_			relatively higher than is characteristic of the device body;				
19	•	(f)	forming an insulating layer over the electrode layer, first lateral region, and second				
20			lateral region;				
21		(g)	electrically connecting the first and second lateral regions to a first supply voltage				
22			potential at a first longitudinal end of the device body; and				
23		(h)	electrically connecting the electrode layer to a second supply voltage potential at a				
24		•	second longitudinal and of the device had a sense its to the first less its direct and				

1		of the device body.
· 2		
3	2.	(Original) The method of Claim 1 wherein the first type of dopant material comprises N-
4	,	type material and the step of forming the device body includes implanting the N-type
5		material in a bulk P-type semiconductor substrate.
6		
7	3.	(Original) The method of Claim 2 further including:
8	•	(a) forming an N-well in the semiconductor substrate prior to forming the device
9		body; and
10		(b) wherein the step of forming the device body includes performing an additional N-
	••	type material implantation in a selected area of the N-well.
13	4.	(Original) The method of Claim 1 further including the step of forming a first end region
14		in the semiconductor substrate abutting the first longitudinal end of the device body and
15		contacting the first and second lateral regions adjacent to the first longitudinal end of the
16		device body, the first end region being formed using the first type of dopant material.
17	· · · .	
18_	5,	(Original) The method of Claim 4 wherein the step of electrically connecting the first
19	•	lateral region and the second lateral region to the first supply voltage potential comprises
20		forming ground potential contacts to the first end region.
21		
22	6.	(Original) The method of Claim 1 further including the steps of forming a buried oxide
23		layer in the semiconductor substrate and forming side oxide regions in the semiconductor

substrate in areas bounding an area for the capacitor, the steps of forming the buried

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.1		oxide layer and side oxide regions being performed prior to forming the device body.
. 2		
3		
4	7.	(Original) The method of Claim 6 wherein the first type of dopant material comprises N-
5		type material and the step of forming the device body includes implanting the N-type
6		material in the volume of the semiconductor substrate defined between the side oxide
7	. *	regions.
. 8		
9	8.	(Original) The method of Claim 7 wherein the step of forming the first and second lateral
10		regions comprises implanting additional N-type material in areas defined between lateral
11	•	sides of the device body and the side oxide regions.
12		
13	9.	(Original) The method of Claim 7 wherein the step of forming the device body includes
14		an additional N-type material implantation in the volume of the semiconductor substrate
15		defined between the side oxide regions.
16	٠	
17	10.	(Original) The method of Claim 7 further including the step of forming a first end region
18	= · · · · · · · · · · · · · · · · · · ·	in the semiconductor substrate abutting the first longitudinal end of the device body and
19		contacting the first and second lateral regions adjacent to the first longitudinal end of the
20	•	device body, the first end region being formed using N-type material.
21		
22	11.	(Original) The method of Claim 10 wherein the step of electrically connecting the first
23		lateral region and the second lateral region to the first supply voltage potential comprises
24	•	forming ground potential contacts to the first end region.

1	12.	(Currently Amended) A method of forming a capacitor on a semiconductor substrate				
2		toget	her with an integrated circuit comprising a plurality of first type circuit devices and a			
3		<u>plura</u>	lity of second type circuit devices, the method including the steps of:			
4		(a)	concurrently forming a capacitor device body and a plurality of additional first			
5		,	type device bodies in the semiconductor substrate using a first type of dopant			
6		•	material, each additional first type device body corresponding to a respective one			
7			of the first type circuit devices;			
8	1)(1	(b)	concurrently forming a dielectric layer over the capacitor device body and over			
9	٠		each additional first type device body;			
10		(c)	concurrently forming an electrode layer over the dielectric layer in an area defined			
1	•		by an upper surface of the capacitor device body and in each respective area			
12	•		defined by an upper surface of each respective additional first type device body;			
13		(d)	forming a first lateral region and a second lateral region in the semiconductor			
1.4 .			substrate along opposite lateral sides of the capacitor device body and			
15			concurrently forming a respective drain region and a respective source region in			
16			the semiconductor substrate along opposite sides of each respective additional			
17		•	device body for a number of the second type circuit devices, the first lateral			
1-8			region, and second lateral region, each respective drain region, and each			
19		,	respective source region being formed using the first type of dopant material at a			
20			level relatively higher than is characteristic of the capacitor device body and each			
21	. *		respective additional device body;			
22		(e)	forming an insulating layer over the electrode layer, first lateral region, second			
23			lateral region, each respective drain region, and each respective source region;			
24		(f)	electrically connecting the first and second lateral regions to a first supply voltage			

· 1			potential at a first longitudinal end of the capacitor device body; and
2		(g)	electrically connecting the electrode layer situated over the upper surface of the
3			capacitor device body to a second supply voltage potential at a second
4			longitudinal end of the capacitor device body opposite to the first longitudinal end
5			of the capacitor device body.
6			
7	13.	(Cur	rently Amended) The method of Claim 12 wherein the first type of dopant material
8		comp	prises N-type material and the step of concurrently forming the capacitor device body
9		and e	each respective additional first type device body includes implanting the N-type
10	1	mate	rial in a bulk P-type semiconductor substrate.
11			
12	14.	(Orig	inal) The method of Claim 12 wherein the step of forming the first lateral region,
13		secon	nd lateral region, each drain region, and each source region also includes
14		conci	arrently forming a first end region in the semiconductor substrate abutting the first
15		longi	tudinal end of the capacitor device body and contacting the first and second lateral
16		regio	ns adjacent to the first longitudinal end of the capacitor device body.
17	,		
18_	15.	(Curr	ently Amended) The method of Claim 12 further including the steps of:
19		(a)	forming a buried oxide layer in the semiconductor substrate, the buried oxide
20			layer being formed in an area for the capacitor and in a respective area for each
21			respective circuit device;
22	÷	(b)	forming a first set of side oxide regions in the semiconductor substrate for the
.23			capacitor, the first set of side oxide regions bounding the area for the capacitor;
24		(c)	forming a respective additional set of side oxide regions in the semiconductor

1		substrate for each respective circuit device, the respective additional set of s	side
2		oxide regions bounding the area for the respective circuit device; and	
3 ·		d) wherein the steps of forming the buried oxide layer and each set of side oxide	de
4		regions are performed prior to forming the capacitor device body and each	
5		additional first type device body.	
6			
7 .	16.	Currently Amended) The method of Claim 15 wherein the first type of dopant mat	erial
8	•	omprises N-type material and the step of forming the capacitor device body and ea	ich
9		ditional first type device body includes implanting the N-type material in the area	ıs of
10		e semiconductor substrate defined within each respective set of side oxide regions	s
11	*	orresponding to the capacitor device body and each first type device body.	
12	. •		٠.
13	17.	he method of Claim 16 wherein the step of forming the first lateral region and sec	ond
14		teral region comprises implanting additional N-type material in areas defined bety	ween
15	•	teral sides of the capacitor device body and the first set of side oxide regions, and	
16		herein the step of forming each drain region and each source region comprises	
17		nplanting additional N-type material for the respective second type circuit devices	<u>in</u>
18		eas defined between lateral sides of the respective additional device body and the	
19		spective additional set of side oxide regions.	
20			
21	18.	Currently Amended) A method for improving the frequency response of a decoupl	ing
22		apacitor in an integrated circuit, the decoupling capacitor including a device body	
23		nalogous to the device body of a first type of transistor included in the integrated of	ircuit

and being formed using a first type impurity material, the decoupling capacitor further

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including first and second l	ateral regions and	logous to the so	ource and drai	n regions of the
a second type of transistor i	included in the in	tegrated circuit	chip, the metl	nod comprising
the step of:			• .	•

(a) adding additional first type impurity material to an area in the substrate for the decoupling capacitor device body located above a buried oxide layer of a siliconon-insulator integrated circuit, the additional first type impurity material resulting in a region on the substrate for the decoupling capacitor device body that is more highly doped than a region on the substrate for the first type of transistor device body.

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- 19. Canceled
- 12 20. Canceled